RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF TECHNOLOGY

BET (Hons) Degree in Electrical and Electronic Technology
Third Year - Semester I Examination January/February 2025

EET 3203 – Computer Systems

Time: Two (02) hours

• Answer all Questions, all questions carry equal marks.

1) Computer memory is a critical component that electronically holds the data and programs the CPU needs for quick access.

a)

i) Describe the operation of the Control Unit, Arithmetic and Logic Unit (ALU), and Registers within the CPU and how they interconnect. **[3 marks]**

ii) *Von Neumann's architecture* is still widely used in modern computers. Describe the important structure of Von Neuman's architecture. **[3 marks]**

b)

i) Briefly explain "*Cache Hit*" and "*Cache Miss*" using appropriate diagrams. **[4 marks]**

ii) What is the main difference between *direct* mapping and *associative* mapping? **[3 marks]**

c) Consider a machine with a byte-addressable main memory of 2^{16} bytes and a block size of 8 bytes. This machine uses a direct-mapped cache with 32 lines.

i) What is the address length? **[2 marks]**

ii) How many bits are needed to represent a cache memory line? **[2 marks]**

iii) How many bits are there in the tag? **[2 marks]**

iv) What is the purpose of the tag in an address? **[2 marks]**

v) What is the size of the cache? **[2 marks]**

vi) How many numbers of blocks are there in this memory? **[2 marks]**

[Total 25 Marks]

2) Processor techniques include various strategies and methods used in CPU design and operation.

a)

i) Briefly explain the technique of "*Branch Prediction*" which is used to improve the performance of a processor. **[3 marks]**

ii) What is meant by "*Performance Balance*"? **[2 marks]**

iii) Suggest a method to increase data transfer speed between the processor and main memory. **[2 marks]**

iv) Identify and describe the factors that limit the processing speed of a CPU. **[2 marks]**

v) Using an appropriate diagram and explain the bus architecture of a computer. **[3 marks]**

b)

i) Briefly explain three (3) performance parameters of a computer memory. **[3 marks]**

ii) Using the concept of memory hierarchy, briefly explain why it is essential to have different types of memory rather than a single type for all purposes. **[3 marks]**

iii) The ***D-RAM*** structure is illustrated in ***Figure 01.*** Identify and explain the operation of the components **A** and **B**. **[2 marks]**

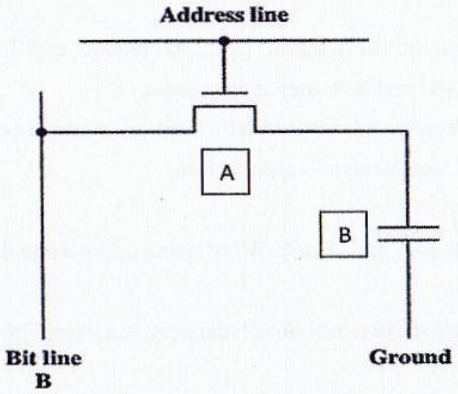

Figure 01: D-RAM Structure

iv) What potential failures could occur in the component B, and explain its impact on ***D-RAM operation***? **[3 marks]**

v) Explain why a periodic charge refreshing is required in ***D-RAM.*** **[2 marks]**

[Total 25 Marks]

3) A computer processor executes instructions, manages tasks and handles interrupts to address urgent events before resuming normal operations. **Table 1** shows the priority of three I/O devices when an interrupt occurs. The table also provides the Time of Occurrence for each device's interrupt measured from the start time (t = 0). Each interrupt requires 10 nanoseconds to handle.

Device	Priority	Time of Occurrence
Communication link	5	t = 10
Printer	3	t = 5
External Memory	2	t = 8

Table 1: List of interrupts

a)

i) What is the purpose of implementing *interrupts* in a computer system? **[2 marks]**

ii) Draw a flowchart showing the processor's operations in the **absence** of an interrupt routine. **[2 marks]**

iii) Draw an *interrupt routine* and explain how the multiple interrupts given in *Table 1* are handled using the **second approach method**. **[5 marks]**

b)

i) Compared to an IAS machine, the most significant change in the second generation of computers is the use of *data channels*. Briefly explain the function of these data channels. **[3 marks]**

ii) Write another significant feature of second-generation computers, apart from the use of data channels. **[2 marks]**

c) Consider an instruction pipeline with 5 stages, a pipeline cycle time of 20ns, and 100 instructions to process. Answer the following questions based on your understanding of instruction pipelining.

i) Briefly explain the process of '*Instruction pipelining*'. **[1 mark]**

ii) List three (3) types of *pipeline hazards*. **[1 mark]**

iii) Calculate the total pipeline time. **[3 marks]**

iv) Calculate the total non-pipeline time. **[3 marks]**

v) Calculate the Speed-up Ratio. **[3 marks]**

[Total 25 Marks]

4) Answer the following questions based on *computer* arithmetic indicating all necessary steps.

a)

i) Convert 324_{10} into binary coded *decimal (BCD)* form. **[2 marks]**

ii) Convert the following decimal numbers into *8-bit two's complement* form.

- 60_{10}
- -36_{10}

[2 marks]

iii) Convert the following *8-bit two's complement* numbers into *decimal* form.

- 01101100_2
- 10011011_2

[2 marks]

iv) Apply the *add-and-shift algorithm* to perform the multiplication of the binary numbers 1110 and 1010. **[4 marks]**

v) Convert 1.32125×2^{-7} into a typical *32-bit floating point* format. **[4 marks]**

b) *RAID memory systems* enhance data storage reliability and performance across multiple disks.

i) What are the key benefits of using a RAID system? **[2 marks]**

ii) List four (04) commonly used RAID Systems. **[2 marks]**

iii) What are the three (03) main techniques used in RAID systems? **[3 marks]**

iv) Based on your understanding, which RAID configuration would you recommend for the storage of E-Books in a university library? Justify your choice by discussing the advantages and disadvantages of the RAID system you selected. **[2 marks]**

v) Discuss the advantages and disadvantages of *Solid-State Drives* (*SSDs*) instead of *Hard Disk Drives* (*HDDs*) for data storage. **[2 marks]**

[Total 25 Marks]

[Question paper 100 marks]

----- End ----